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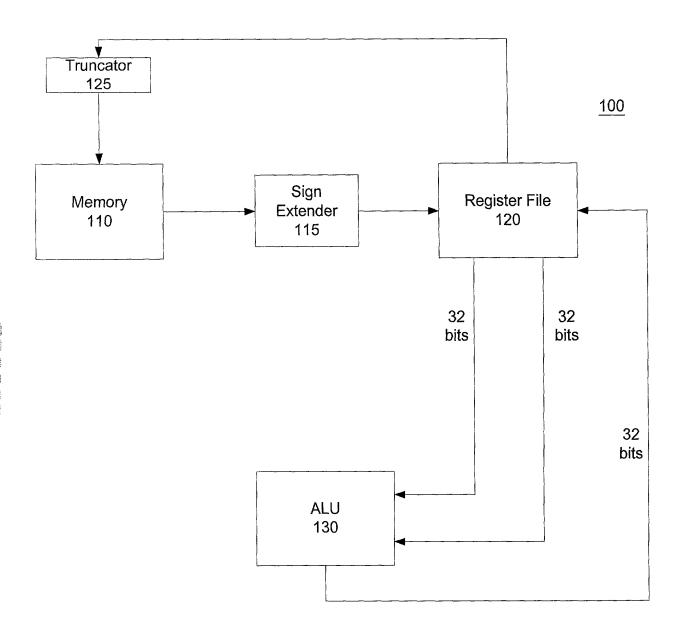


Figure 1A

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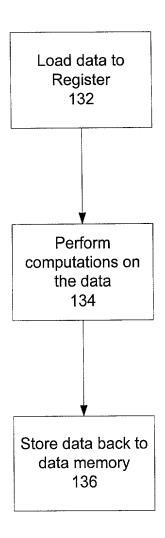


Figure 1B

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OPCode 6 bits	ource1 Source2 egister Register bits 5 bits	Target Register 5 bits	Sub-OPCode 11 bits
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Figure 1C

OPCode 6 bits	Target Register 5 bits	Source1 Register 5 bits	Immediate 16 bits
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Figure 1D

200

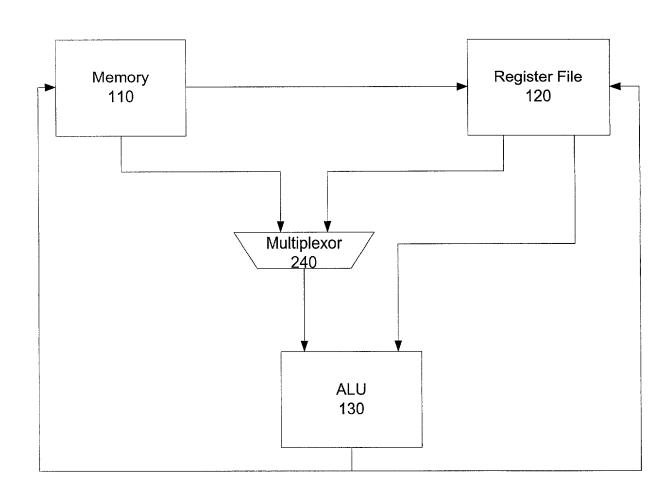


Figure 2

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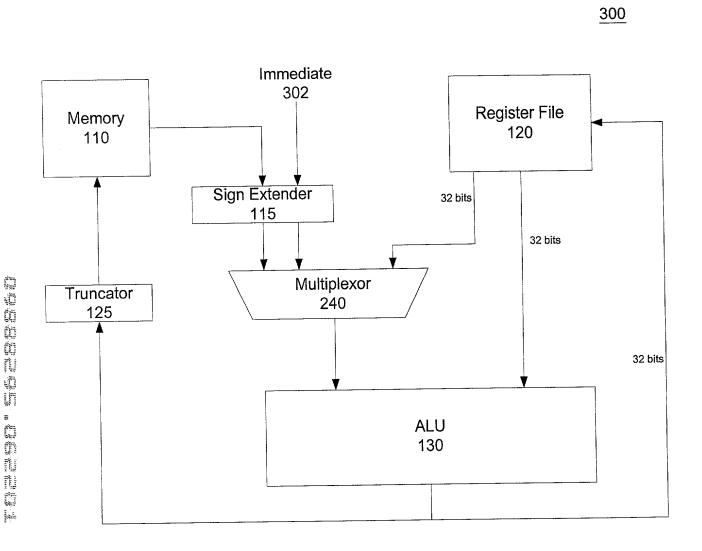
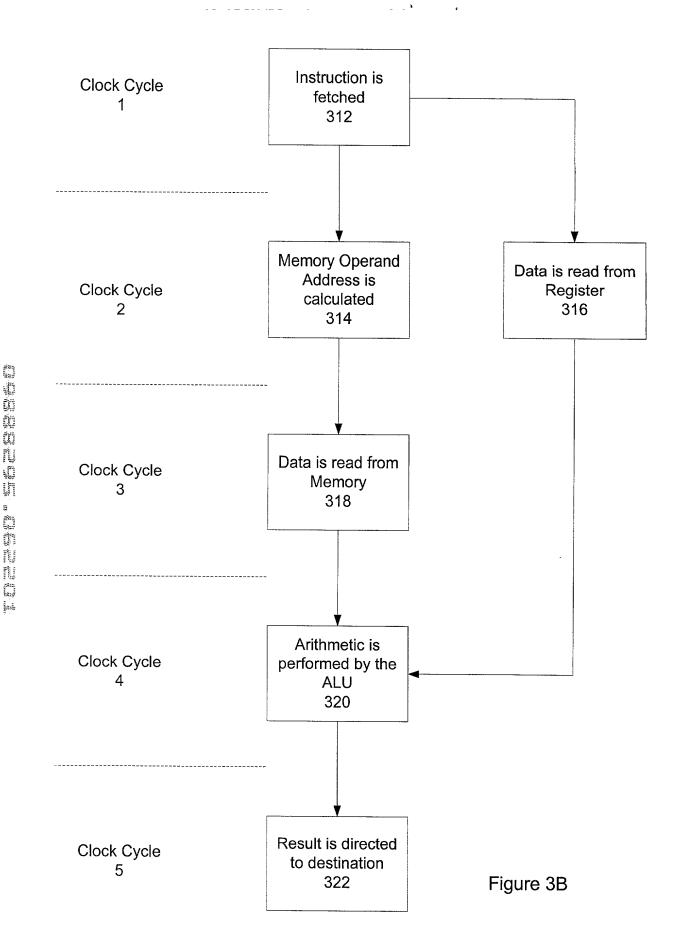


Figure 3A



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<u>400</u>

OPCode 5 bits	Destination 11 bits	Source2 Register 5 bits	Source

Figure 4

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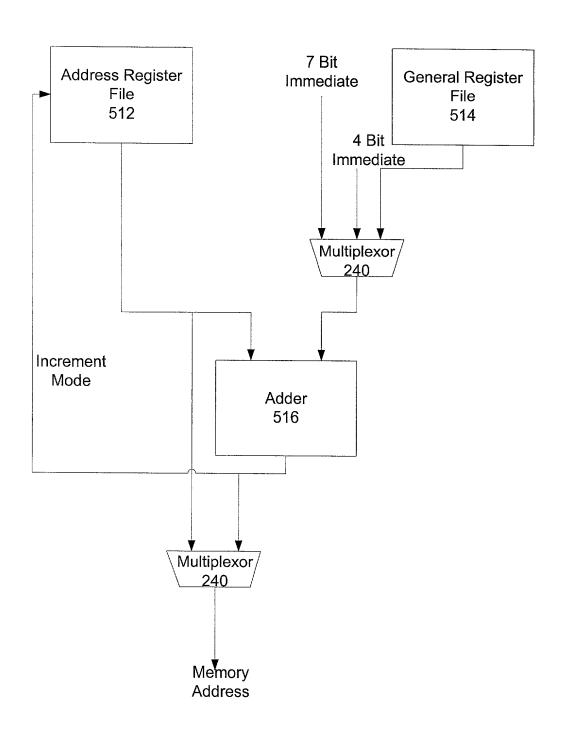


Figure 5

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1 .\_ . .

1	I <sub>6</sub>	l <sub>5</sub>		$\begin{bmatrix} I_4 & I_3 & I_2 & I_1 & I_0 \end{bmatrix}$	Row 1
0	1	1	$A_2A_1A_0$	$R_4 R_3 R_2 R_1 R_0$	Row 2
0	1	0		M l <sub>3</sub> l <sub>2</sub> l <sub>1</sub> l <sub>0</sub>	Row 3
0	0	1	Register Direct		Row 4
0	0	0	Immediate		Row 5

Figure 6

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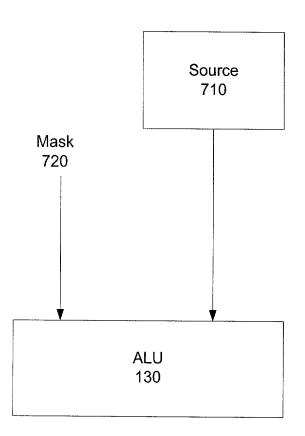


Figure 7

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Word 1 Word 2 Load Shift & Merge

Figure 8

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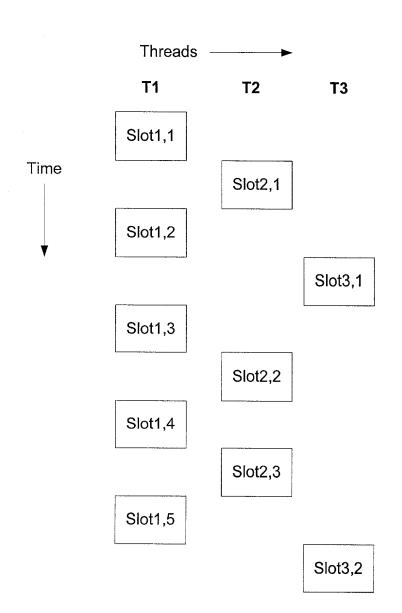


Figure 9